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Digital Control algorithm for Two-Stage DC-DC Converters

Lankala Mounika, Mr. Merugu Anand Kumar, Nagam Aanjaneyulu, **Dr. Inaganti Shylaja**

Associate Professor[1,2,3], Professor[4]

lankala.mounikareddy@gmail.com[1],meruguanand502@gmail.com[2],
anji.amrexamcell@gmail.com[3],shyalajainaganti@gmail.com[4]

Department of CSE, A.M. Reddy Memorial College of Engineering and Technology, Petlurivaripalem, Narasaraopet, Andhra Pradesh

Abstract

The two-stage dc-dc converter's construction process is shown, and a methodical digital management technique is suggested for it. The dynamic reaction of the structure is very complicated because of the large number of reacting components. The steady-state study is used to check the two-stage converter's development. The fleeting reaction of the structure must be analysed, and a tiny signal model is required for this. The system is then adjusted with the help of a computer device that acts as a latency adjuster. Overshoot is reduced and stability is achieved by increasing the crossover frequency relative to the uncompensated converter and improving the second resonant frequency. The design process and the digital controller's steady-state and intermittent excellent characteristics are demo nitrated with experimental data.

Introduction

Wind, nuclear, solar, and other forms of renewable energy[1] are on the rise in popularity and could provide viable solutions to the world's energy problems. However, due to the unreliability of green power generation, energy transmission based on switching management is necessary to obtain reliable and readily accessible power [2]. High input voltage, low voltage/high current output dc-dc conversion is ideally suited to the two-stage dc-dc converter. A buck constitutes the first step of the structure, while a forward, push-pull, half-bridge, or full-bridge may constitute the second. The output of the buck-and-half bridge converter suggested in this article is managed by a 16-bit microcontroller from Freescale. Given that the two duty ratios of the half bridge are both 50%, the second converter is essentially a dc rectifier. After the first stage, the input voltage Vg should drop to and the second stage's output voltage should be.

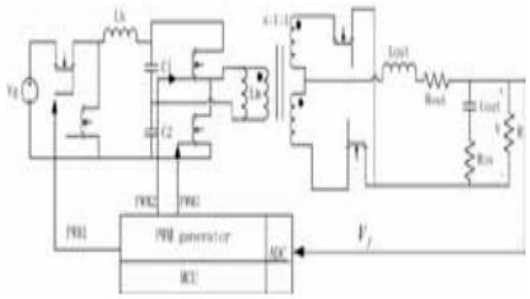

Fig. 1.two-stage dc-dc converter system

The power stage design and feedback loop are standard components of dc-dc systems. It is preferred that this feedback system be designed so that the output voltage is precisely controlled and is not affected by fluctuations in the input current [3]. The output voltage is measured by the ADC of the MCU, and the MCU then uses a mitigate method to adjust the PWM duty ratio of the PWM generator in order to maintain a steady voltage output and a high degree of dynamic reaction (see Fig.1). This This article shows the control method for a digital MCU to two-stage conversion and introduces ac tiny signal analysis. The best way to learn about a two-stage dc-dc converter is through the study of its management mechanism.

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Small signal analysis and modelling

As the topology of the circuit is a no-linear system, and in order to optimize the frequency response of the two-stage converter, an ac small-signal model is necessary. The power stage of the two-stage dc-dc converter can be approximated to an equivalent circuit in Fig 2(a). Where the input voltage Vg, the inductor Lb, and the capacitor C1 and C2 of first stage are converted to , and in the secondary side of the transformer. And their relationships are in (1).

$$L_{buck} = L_b/(2n)^2,\ C_{buck} = 2n^2 C_1,\ V_s = V_g/2n$$

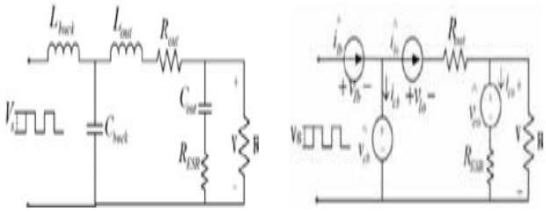

Fig.2. (a) simplify equivalent two-stage dc-dc converter; (b) analytical circuit

Fig.2(b) shows the analytical model which replaced inductor in the constant current source and capacitor in the constant voltage source [4]. The analytical circuit can be modelled by the stage-space average approach method in [5]. Furthermore, the transfer function of the converter will be got. Here, the x(t) is a vector containing the four state variables, that is, the inductor currents, and the capacitor voltage ,. The input vector u(t) contains the independent inputs and in this system is in (3). Using the circuit analysis theory to the analytical circuit, the state space equations are set up in (4).

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}$$

$$\mathbf{B} = \begin{bmatrix} 0 & 0 & 0 & D/L_b \end{bmatrix}^T \quad \mathbf{x} = \begin{bmatrix} V_{cb} & i_{lb} & V_{co} & i_{lo} \end{bmatrix}^T \quad u = V_s$$

$$\mathbf{A} = \begin{bmatrix} 0 & 1/C_{buck} & 0 & -1/C_{buck} \\ -1/L_{buck} & 0 & 0 & 0 \\ 0 & 0 & -1/C_{out}(R_{ESR}+R) & R/C_{out}(R_{ESR}+R) \\ 1/L_{out} & 0 & 1/(L_{out}(R_{ESR}+R) & -(R_{out}+R\|R_{ESR})/L_{out} \end{bmatrix}$$

From the dynamic (ac) model, the state variable to the control transfer function can be derived in (5). Four variables are substituted into (5), there will be four equations could be got, and here just use one (6).P(s) is derived from , and is also can be got in (9), so the control to output transfer function is clearly in (10). And use the (10), the control to output transfer function can be derived.

$$\frac{\hat{\mathbf{x}}(s)}{\hat{d}} = (s\mathbf{I} - \mathbf{A})^{-1}\frac{\partial \mathbf{B}}{\partial D} \bullet V_s$$

$$G_{V_{cod}}(s) = \hat{V}_{co}/\hat{d}(s) = G_{V_{co}}(s)/P(s)$$

$$P(s) = s^4 L_{buck}L_{out}C_{buck}C_{out}(R+R_{ESR}) + s^3(L_{buck}L_{out}C_{buck} + L_{buck}C_{buck}C_{out}RR_{ESR}) + s^2$$
$$[L_{out}C_{out}(R+R_{ESR}) + L_{buck}C_{buck}R + L_{buck}C_{out}(R+R_{ESR})] + s(L_{buck} + L_{out} + RC_{out}) + R$$

$$G_{V_{co}}(s) = R$$

$$G_V(s) = RV_s(1 + sC_{out}R_{ESR})$$

$$G_{Vd}(s) = \hat{V}(s)/\hat{d}(s) = G_V(s)/P(s)$$

Digital-controller design

A small signal model has been made in the former section, in order to get the control to output transfer function, it should substitute the parameters (table 1) into (1), (7), (9) and (10). This dc-dc converter is designed: input voltage is 100v-200vDC, and the output constants 13v. In the table.1, a specific dc-dc converter is used to valid the goodness feature of the two stage dc-dc converter in full digital controller.

Parameter name	Symbol	Nominal Value
First stage inductor		100uH
First stage capacitor		4.7uF
Output inductor		20uH
Output capacitor		2mF
Series resistance of the secondary side		200mΩ
Equivalent series of the output capacitor		10mΩ
Turn ratio of the transformer	n	4
Input voltage		144v

Using the parameters of table.1, a control to output transfer function can be got. And its frequency characteristic is derived in Fig 3(a).

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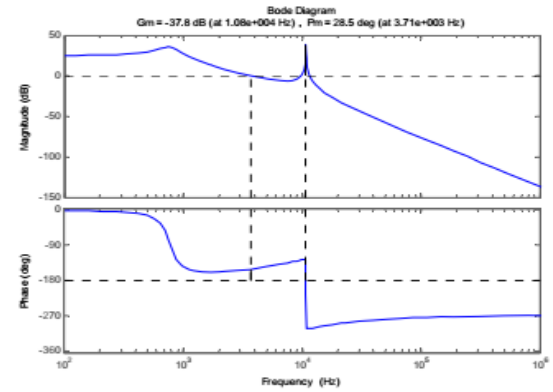

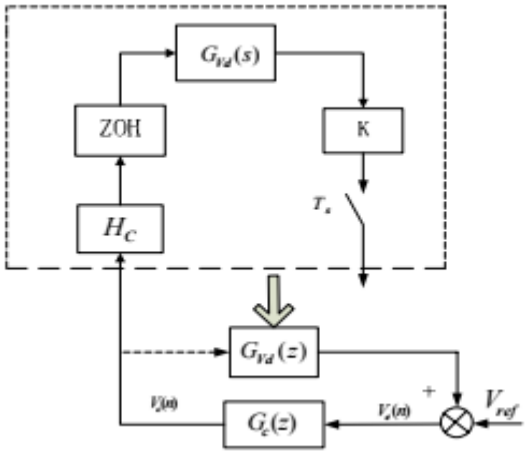

Fig. 3(a) bode plot of the control-to-output transfer function; (b) the diagram of digital control The bode plot of the control to output transfer indicts it is a fourth order system: combined by one zero and two conjugate poles which lead to two system resonances, and its phase shifts to at high frequency. Magnetizing inductance does not affect the dynamics because half bridge is operating constantly with d=50% and the resonance between Lam and capacitor C does not appear [6]. Analysis shows that the first resonance frequency is mainly determined by, and, while the second resonance frequency is mainly determined by, and [7].So the controller is designed to increasing the second resonance frequency as to achieve a higher bandwidth

digital control analyses

Generally, the controller of the dc-dc converters is designed in s-domain, and it is widely applied in the

analogy controllers and some digital controllers. But this time the two-stage dc-dc converter is designed in z-domain, which the delay of the sampling and holds in MCU is considered. The main block diagram is in figure 3(b). From the Fig 3(b), the K is the proportion of the sensor, is the compute delay of the MCU, which include the delay of AD conversion, ZOH is the zero-order sampled hold of the DPWM and AD conversion, is the controller which is designed. The sampling and holds transfer function in s-domain is in (11). The compute delay contains the delay time of the AD conversion and the date update time of PWM generator. If all of delay time is

denoted by, they can be expressed in (12).

$$SH(s) = (1 - se^{-sT_s})/s$$

$$H_c(s) = e^{-sT_d}$$

$$G_{Vd}(z) = Z\{\frac{1 - se^{-sT_s}}{s} \cdot H_c(s) \cdot G_{Vd}(s) \cdot K\}$$

In the design of direct digital control system, the power stage model should be discrete first. Substitute the equations (10)-(12) into (13), the discrete transfer function is derived in the case of delay Td=0 in (14). Using MATLAB control toolbox 'SISOTOOL', a compensate transfer function (15) is got through the direct digital control method and it is a lag compensator.

$$G_{Vd}(z) = \frac{0.01391z^3 + 0.05444z^2 - 0.001828z - 0.007425}{z^4 - 2.242z^3 + 2.583z^2 - 2.139z + 0.8106}$$

$$G_c(z) = \frac{0.036337(z - 0.6385)}{z - 1}$$

So, the expression of the discrete in z-domain can be derived in (16). Its bode plots of the compensated system is in Fig 4(a).

$$u(k) = u(k-1) + 0.036e(k) - 0.0234e(k-1)$$

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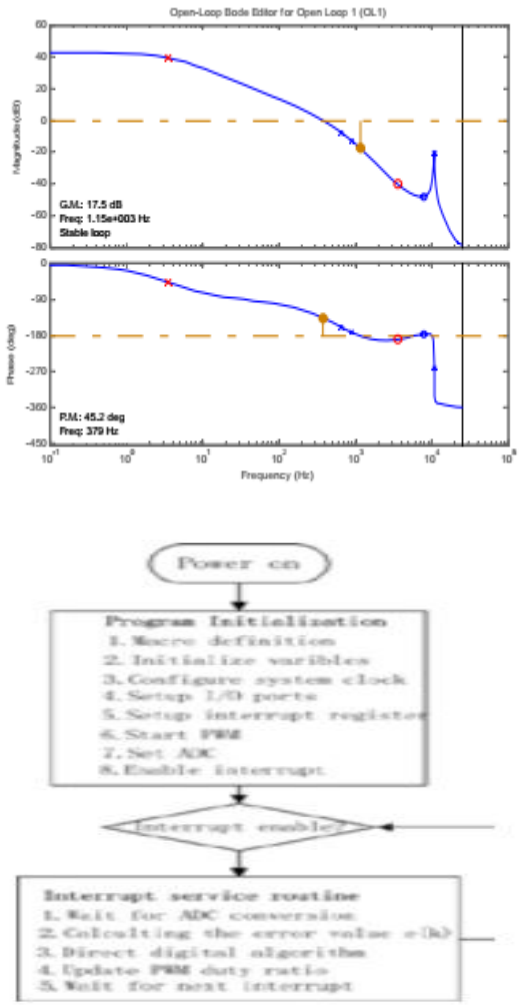

Fig. 4(a) the plot of compensated bode; (b) the main progress of the control algorithm in MCU

The workflow of the digital controller

The complete digital controller implement in the MCU is interrupt driven. The PWM module loads the new value of duty cycle at the beginning of every switching cycle. All the calculations of the digital control algorithms are applied in the ADC interrupt service routine. The main progress of the control algorithm is represented in the flow chat in figure 4(b).

Experimental results

This section evaluates the performance of the digital controller for two-stage-converter designed using the procedure described in the previous section, which is a lag compensator. Fig 5(a) displays the output waveforms of the converter operating with the input voltage of 144v in the control of the digital lag algorithm in MCU, the output voltage constants 13V. From the Fig 5(a), the output is display the goodness steady-state waveform which is desired.

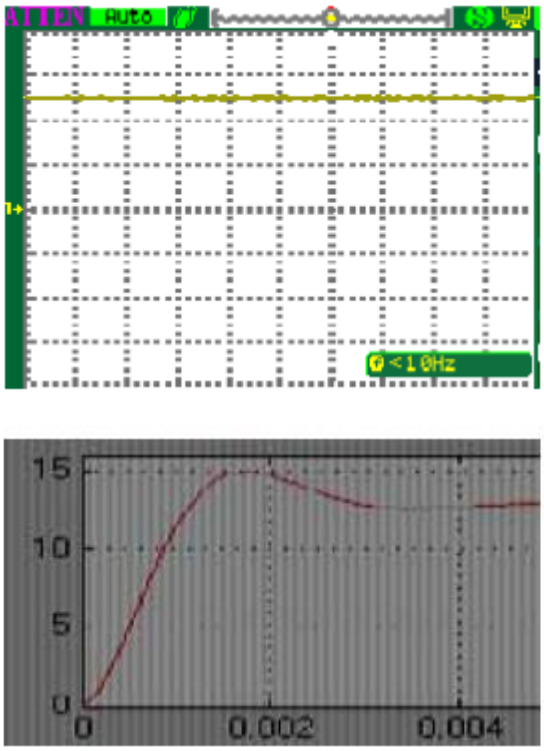

Fig. 5(a) Waveforms of output voltage at steady-state operation V=13v; (b) the simulated waveform of the startup of the two-stage converter with the digital controller The evaluation of the transient response is done to analysis the stability of the model and its high speed response. In order to evaluate the transient response, the startup of the two-stage converter is simulated. The transient of the two-stage converter is with digital Lag compensate controller behave a good response in Fig 5(b).

Conclusion

This article proposes using a digital processor to manage the two-stage dc-dc conversion. Both the large- and small-signal topology theories are examined in depth. The brains of the device are an MCU, making it a computerized instrument. To get the intended results from the feedback loop, a lag buffer is introduced to the forward route. The management is planned around the microcontroller's latency. algorithm. Based on the findings of the experiments, a digital control method to increase the bandwidth of the uncompensated converter is feasible. Improvements were made to both the constant and fleeting responses. The testing

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outcomes validate the structure and management approach of the two-stage conversion system. Since there are limitations to the single-voltage method of control as well, efforts will be directed toward developing a two-loop control scheme that takes into account the inductor's current for a more responsive dynamic range.

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